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Sheet 1 of 1

Complete if Known

Application Number	Not yet assigned
Filing Date	June 27, 2001
First Named Inventor	RAKVIC et al
Group Art Unit	Not assigned
Examiner Name	Not assigned
Attorney Docket Number	2207/111236

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U.S. PATENT DOCUMENTS

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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
AMI		Rivers et al, "On High-Bandwidth Data Cache Design for Multi-Issue Processors", IEEE, Proceedings, Micro-30, Dec. 1-3, 1997, Research Triangle Park, North Carolina	
MI		Neefs et al, "A Technique for High Bandwidth and Deterministic Low Latency Load/Store Accesses to Multiple Cache Banks, 6th Int'l. Symposium on High-Performance Computer Architecture HPCA-6, IEEE, 1999, Los Alamitos, California	
MI		Calder et al, "Predictive Sequential Associative Cache", IEEE, Proceedings 2nd Int'l. Symposium on High-Performance Computer Architecture, Feb. 3-7, 1996, San Jose, California	
MI		Cho et al, "Decoupling Local Variable Accesses in a Wild-Issue Superscaler Processor, Proceedings of the 26th Annual Int'l. Symposium on Computer Architecture, May 1999	

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